REMARKS

Applicant respectfully request reconsideration and allowance of the present application in view of the following remarks. Claims 24-35 are pending in the application.

Objections to the Drawings

The drawings stand objected to for informalities. By this Amendment, Applicant proposes to conform FIG. 4 to the specification by adding reference labels for OUTN and OUTP (page 13, line 14 and page 14, line 7 of the disclosure).

Applicant provides herewith a corrected drawing as required by the Examiner. Applicant requests entry of Figure 4 as shown on the Replacement Sheet attached as the Appendix to this reply. Applicant will provide formal drawings upon approval of the amendments by the Examiner.

For the foregoing reasons, the objections to the drawings should be withdrawn.

Claim Rejections Under 35 U.S.C. § 103

Claims 24, 25, 26, 27, 30 and 34-35 stand rejected as allegedly being unpatentable under 35 U.S.C. § 103(a) over U.S. Patent No. 4,520,324 to Jett et al. (hereinafter "Jett") in view of U.S. Patent No. 5,313,172 to Vagher (hereinafter "Vagher"). Claims 28-29 and 31-32 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Vagher in view of Jett and further in view of U.S. Patent No. 6,201,443 to Tanji ("Tanji"). Claim 33 stands rejected under 35 U.S.C. § 103 as being unpatentable over Jett in view of Vagher and further in view of U.S. Patent No. 5,313,172 to Yun ("Yun"). Applicant respectfully traverse the rejections for at least the reasons set forth below.

Applicant respectfully submits that the rejections of the claims in the present Application are based on a misapprehension of the cited references. Applicant restates the prior arguments made in response to previous Office Actions in this Application and provides the following additional remarks to facilitate a better appreciation of the deficiencies in the cited references with respect to the claimed inventions.

Independent Claim 24 Patently Defines Over Jett and Vagher

A *prima facie* case of obviousness under § 103 requires that each and every limitation be taught or suggested in the cited prior art. MPEP 2143.03; *In re Royka*, 490 F.2d 981 (CCPA 1974).

In the Office Action, the Examiner maintains the contention that Vagher teaches "a digitally switched gain amplifier with a plurality of gain cells, each gain cell coupled to the input current load circuit and receiving the output differential signal..." Applicant respectfully submits that this contention derives from a misapprehension of the cited drawing and description in Vagher. For example, the Examiner cites transistors Q30, Q32, Q34 and Q36 in suggesting that Vagher teaches or renders obvious "a plurality of gain cells, each gain cell coupled to the input current load circuit and receiving the output differential signal, each gain cell comprising two current mirror circuits," as required by claim 24. However, the cited drawing and associated description do not support the Examiner's suggestion. For convenience, FIG. 3 of Vagher is reproduced below.

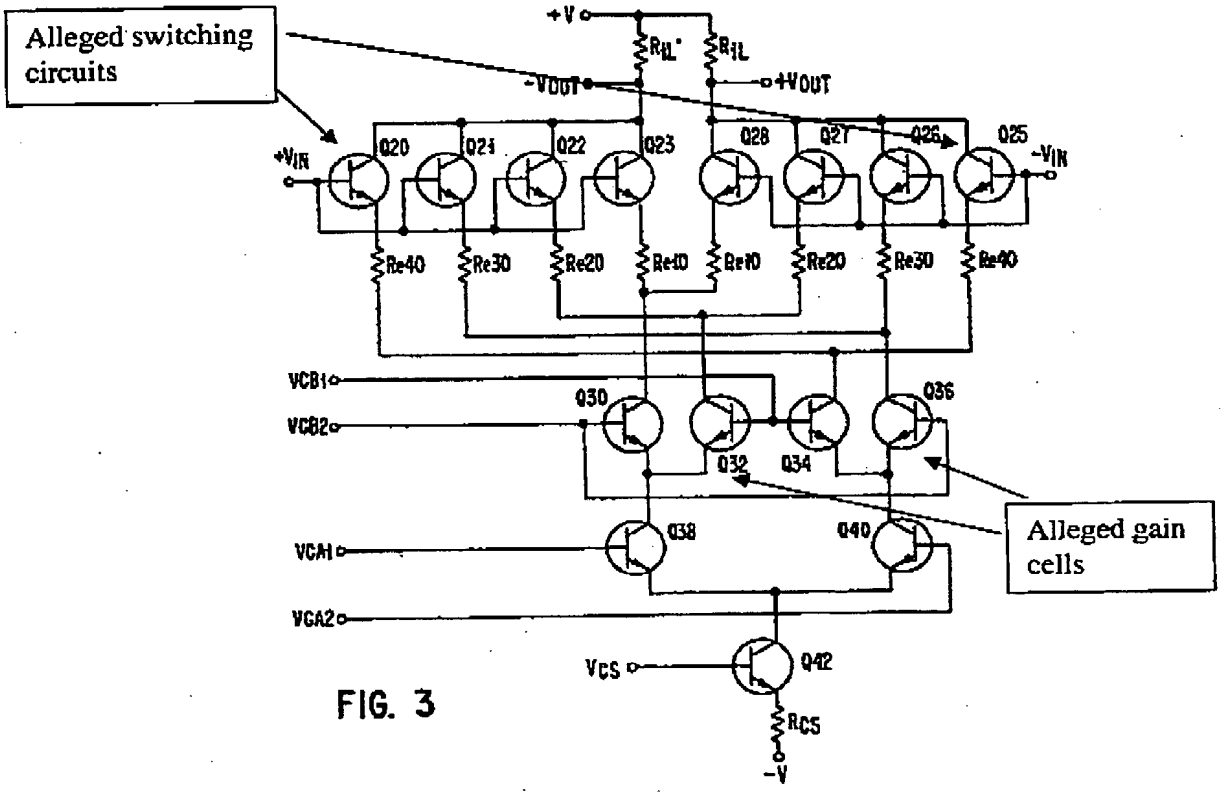


FIG. 3

Specifically, transistor pairs Q30/Q32 and Q34/Q36 are used to turn on respective differential amplifiers for selecting one of four gains (col. 5, lines 6-11). Consequently Q30, Q32, Q34 and Q36 cannot be construed as gain cells. Nor can these transistors be posited as pairs of current mirror circuits because no current mirror circuits are depicted, described or even suggested in Vagher. Therefore, these transistor pairs in Vagher cannot be reasonably said to correspond to a "plurality of gain cells, each gain cell coupled to the input current load circuit and receiving the output differential signal, each gain cell comprising two current mirror circuits," as required by claim 24.

Next the Examiner alleges that transistor pairs Q20/Q25, Q21/Q26, etc. in Fig. 3 of Vagher teach "a plurality of switching circuits, each switching circuit coupled to one of the plurality of gain cells and each switching circuit operating in a positive mode and in a negative mode, the negative mode having an opposite polarity of the positive mode, and wherein the plurality of switching circuits operate to place more of the plurality of gain cells in the positive mode than in the negative mode," as recited in Claim 24. This allegation is misguided. A review of Vagher as cited reveals that transistors Q20-Q28 are used as simple transistor amplifiers with respective gains determined by emitter resistors Re10, Re20, Re30 and Re40 (*see* Figure 3 and col. 4, line 60 – col. 5 line 13). Further, Vagher does not teach or suggest placing gain cells in a positive mode or negative mode. It is apparent, therefore, that these transistor pairs in Vagher cannot possibly correspond to a plurality of switching circuits, each switching circuit coupled to one of the plurality of gain cells and each switching circuit operating in a positive mode and in a negative mode, the negative mode having an opposite polarity of the positive mode, and wherein the plurality of switching circuits operate to place more of the plurality of gain cells in the positive mode than in the negative mode, as required by claim 24.

It is apparent that the rejections in the Office Action are based on a misinterpretation of the structure and operation of the circuit in Figure 3 of Vagher. Specifically, amplifying transistors Q20-Q23 and Q25-Q28 have been ascribed the function of switches while switching transistors Q30, Q32, Q34 and Q36 have been misconstrued as amplifiers or gain cells. As shown above, at best, a reverse interpretation of these transistors is appropriate. Nevertheless, Applicant respectfully submits that Vagher, even if interpreted correctly, would not have anticipated or rendered obvious the subject matter of the present Application.

Independent claim 24 requires a plurality of gain cells, each gain cell coupled to the input current load circuit and receiving the output differential signal, each gain cell comprising two current mirror circuits. In Vagher, each transistor pair of Q20-Q23 and Q25-Q28 is an element of an amplifier with a gain determined by respective emitter resistors and a common collector resistor. Even assuming arguendo that each transistor pair of Q20-Q23 and Q25-Q28 may be regarded as a gain cell, none of these "gain cells" comprise two current mirror circuits. Further, no combination of transistors Q20-Q23 and Q25-Q28 can be said to comprise two current mirror circuits. Therefore, Vagher fails to anticipate or render obvious the gain cells comprising two current mirror circuits as recited in claim 24.

Independent claim 24 further requires a plurality of switching circuits, each switching circuit coupled to one of the plurality of gain cells and each switching circuit operating in a positive mode and in a negative mode, the negative mode having an opposite polarity of the positive mode. Assuming once more arguendo that each transistor pair of Q20-Q23 and Q25-Q28 may be regarded as an amplifier or gain cell, the circuit of Figure 3 still does not have gain cells that can be placed in a positive mode and in a negative mode as required by claim 24. The gain of each of the amplifiers of Figure 3 is switched between a predetermined gain and no gain by a combination of switches associated with transistors Q30, Q32, Q34 and Q36 (paragraph spanning cols. 4 and 5). It is apparent that these switches are of a binary nature, being configured to select whether a differential amplifier is to be turned on or off (paragraph spanning cols. 4 and 5). No negative mode and positive mode switches are taught in Vagher. Consequently, Vagher fails to anticipate or render obvious the plurality of gain cells placed in the positive mode than in the negative mode recited in claims 24.

Therefore, even if interpreted correctly, Vagher would not have anticipated or rendered obvious the subject matter of the present Application.

Turning now to Jett, in the Office Action the Examiner maintains that the circuit presented in Fig. 3 of Jett anticipates an inductively loaded folded cascode circuit that inputs an input differential signal having a Voltage Drain-Drain (VDD)-referenced output level and outputs a current. Applicant disagrees. The Examiner further argues that Jett's system will "output a voltage and a current when connected." Ohm's law notwithstanding, Applicant respectfully submits the circuit in Figure 3 of Jett produces an amplified voltage output at

terminals 21 and 21', the output voltage being measurable across the connected ***output load device 19*** (Figure 3 and col. 3, lines 23-44). That the output is a voltage is confirmed considering: (1) the circuit in Figure 3 is intended to produce an amplified version of input signal 17 and 17' (col. 3, lines 20-44); and (2) input signals 17 and 17' are voltages applied to the ***gates*** of transistors 12 and 12' respectively (*see* Figure 3, esp. elements referenced at 17 and 17' and labeled "V"). Jett does not support an argument that an additional connection would enable the circuit of Figure 3 to produce the output current required by Claim 24. Therefore, it cannot reasonably be said that Jett teaches an inductively loaded folded cascode circuit that inputs an input differential signal having a Voltage Drain-Drain (VDD)-referenced output level and outputs a current as required in Claim 24.

For at least these reasons, the rejection of Claim 24 is improper and should be withdrawn. Applicant respectfully submits that the remaining rejections in the Office Action are also improper because the rejections are based on the misapprehensions of the teachings of Jett and Vagher as discussed above.

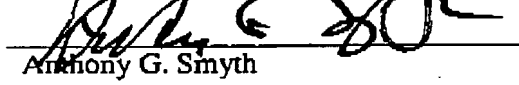
Therefore, for at least these reasons, Applicant respectfully submits that the claims of the present invention are allowable over the prior art and that the rejections should be withdrawn.

Conclusion

All objections and rejections having been addressed, it is respectfully submitted that the present application is in a condition of allowance and a Notice to that effect is earnestly solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

Respectfully submitted,
PILLSBURY WINTHROP LLP

Date: August 15, 2005



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